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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,319	02/14/2002	W. James Allen	DP-305970	8681

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DELPHI TECHNOLOGIES, INC.
M/C 480-410-202
PO BOX 5052
TROY, MI 48007

EXAMINER	
DUNCAN, MARC M	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,319	ALLEN ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *1-6,12,15-19,21,23-32,36,37 and 39* is/are rejected.

7)☐ Claim(s) *7-11,13,14,20,22,33-35 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1-6, 12, 15-19, 21, 23-32, 36-37 and 39 are rejected under 35 U.S.C. 103(a).

Claims 7-11, 13-14, 20, 22, 33-35 and 38 are objected to.

Claim 40 is allowed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 5, 6, 12, 15, 16, 17, 18, 19, 23, 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards et al. in view of Bidner et al.

Regarding claim 1:

Edwards teaches a central processing unit (CPU) coupled to a port which couples the CPU to an external tool in Fig. 1. The processor is coupled through the debug circuit to an external system.

Edwards teaches a volatile memory coupled to the CPU in Fig. 2 "214" and "226" and in col. 5 lines 53-54.

Edwards teaches a state machine in communication with the CPU, wherein the state machine functions to selectively capture information available on an internal bus of the CPU on a cycle-by-cycle basis and store the captured information in the volatile memory in col. 4 lines 1-2, col. 7 line 28, col. 8 lines 6-7 and lines 12-14.

Edwards does not explicitly teach the CPU executing a control algorithm which controls a subsystem coupled to the ECU; a non-volatile memory bank coupled to the CPU, the non-volatile memory bank storing a plurality of calibration tables and a code set. Edwards does, however, teach the CPU running program codes and teaches memories other than those pictured.

Bidner teaches the CPU executing a control algorithm which controls a subsystem coupled to the ECU in Fig. 1, paragraph 0020 and paragraph 0021 lines 1-2.

Bidner teaches a non-volatile memory bank coupled to the CPU, the non-volatile memory bank storing a plurality of calibration tables and a code set in Fig. 1 and paragraph 0022. The processor runs program instructions and therefore the controller memory must inherently include a code set.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the ECU of Bidner with the IC of Edwards.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the ECU of Bidner is an IC or microcontroller used to control the subsystems of a vehicle. The IC of Edwards allows for a trace to be performed in order to ascertain whether the processor of the IC or microcontroller is functioning properly, an inherent need of any such safety critical system.

Regarding claim 2:

Edwards teaches wherein the captured information includes one of a full trace and limited trace of information on at least one of an address and data bus of the CPU in col. 2 lines 17-20 and lines 27-29.

Regarding claim 5:

Edwards teaches wherein the state machine performs triggering, data acquisition and circular buffer control of a trace buffer located within the volatile memory in col. 2 lines 64-65 and col. 7 lines 28-32. The state machine of Edwards extracts the trace info and formats the trace message and then sends the trace information to a circular trace buffer.

Regarding claim 6:

Edwards teaches wherein the state machine includes a counter in Fig. 2. There are multiple counters present in the debug circuit of figure 2.

Regarding claim 12:

Edwards teaches further including: a debug port, wherein the debug port is coupled to the CPU in Fig. 1. The link to the external debug tool is equivalent to a debug port and it can be seen that the CPU is connected to the external port.

Regarding claim 15:

Bidner teaches wherein the CPU, non-volatile memory bank, volatile memory and state machine are implemented within a microcontroller unit (MCU) in Fig. 1 "EC." The EC of Bidner is equivalent to a microcontroller unit.

Regarding claim 16:

Edwards teaches a watchpoint generator for providing a triggering signal to the state machine in col. 10 lines 49-51.

Regarding claim 17:

Edwards teaches a watchpoint generator for providing triggering signals to the state machine in col. 10 lines 49-51.

Regarding claim 18:

Edwards teaches herein the captured information is confined to a specific list by the state machine in col. 2 lines 49-50. Filtering trace information entails confining the capture information to a specific list, i.e. filters.

Regarding claim 19:

Edwards teaches wherein the captured information is confined to an address range specified by the state machine in col. 11 lines 30-42.

Regarding claim 23:

Edwards teaches wherein the state machine captures an address of a CPU access in a specified address range in col. 11 lines 30-42.

Regarding claim 24:

Edwards teaches wherein the state machine stores the captured address in a specific register in col. 3 lines 24-25. Edwards teaches trace information stored in the FIFO, and further teaches the FIFO being composed of memory-mapped registers. The trace information is therefore stored in a specific register, said register being one of the registers of the FIFO.

Regarding claim 25:

Edwards teaches wherein the state machine stores the captured address in the volatile memory in col. 4 lines 1-2.

Regarding claim 26:

Edwards teaches wherein the state machine stores the captured addresses in the volatile memory as a series of packets in col. 8 lines 62-63.

Claims 27, 28, 31, 32, 36, 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards and Bidner as applied to claim 1 above, and further in view of IBM.

Regarding claim 27:

The teachings of Edwards and Bidner are outlined above.

Edwards and Bidner do not explicitly teach an overlay memory coupled to the CPU. Edwards and Bidner do not explicitly teach storing captured information in the overlay memory. Edwards and Bidner do, however, teach a FIFO connected to the CPU, wherein the FIFO is configured as a circular buffer and is used to store the captured information.

IBM teaches an overlay memory on page 488, definition 1.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the overlay memory of IBM with the trace information storage of Edwards and Bidner.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Edwards and Bidner teach organizing the trace information storage as a circular buffer, which creates a need for a memory that uses the same area of storage repeatedly by overwriting the area with new information. The overlay memory of IBM meets this need.

Regarding claim 28:

Edwards teaches wherein the captured information includes one of a full trace and limited trace of information on at least one of an address and data bus of the CPU in col. 2 lines 17-20 and lines 27-29.

Regarding claim 31:

Edwards teaches wherein the state machine performs triggering, data acquisition and circular buffer control of a trace buffer located within the volatile memory in col. 2 lines 64-65 and col. 7 lines 28-32. The state machine of Edwards extracts the trace info and formats the trace message and then sends the trace information to a circular trace buffer.

Regarding claim 32:

Edwards teaches wherein the state machine includes a counter in Fig. 2. There are multiple counters present in the debug circuit of figure 2.

Regarding claim 36:

Edwards teaches a debug port, wherein the debug port is coupled to the CPU in Fig. 1.

Regarding claim 37:

Edwards teaches wherein the port is a debug interface in Fig. 1.

Regarding claim 39:

Bidner teaches wherein the CPU, non-volatile memory bank, volatile memory and state machine are implemented within a microcontroller unit (MCU) in Fig. 1 "EC." The EC of Bidner is equivalent to a microcontroller unit.

Claims 3 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards, Bidner and IBM as applied to claims 2 and 27 above, and further in view of Wood et al.

Regarding claims 3 and 29:

The teachings of Edwards, Bidner and IBM are outlined above.

Edwards, Bidner and IBM do not explicitly teach wherein the CPU has separate instruction and data buses. Edwards, Bidner and IBM do, however, teach a CPU.

Wood teaches wherein the CPU has separate instruction and data buses in col. 3 lines 61-65.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the buses of Wood with the CPU of Edwards, Bidner and IBM.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the CPU of Edwards, Bidner and

IBM inherently needs to transfer instructions and data. The buses of Wood meet such a need.

Claims 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards, Bidner and IBM as applied to claims 2 and 27 above, and further in view of Yamada.

The teachings of Edwards, Bidner and IBM are outlined above.

Edwards, Bidner and IBM do not explicitly teach wherein the CPU uses the same bus for both instructions and data. Edwards, Bidner and IBM do, however, teach a CPU.

Yamada teaches wherein the CPU has separate instruction and data buses in col. 3 lines 34-52.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the bus of Yamada with the CPU of Edwards, Bidner and IBM.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the CPU of Edwards, Bidner and IBM inherently needs to transfer instructions and data. The bus of Yamada meets such a need.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards, Bidner and IBM as applied to claim 1 above.

The teachings of Edwards, Bidner and IBM are outlined above.

Edwards, Bidner and IBM do not explicitly teach protecting the volatile memory from data loss during normal operation. Edwards, Bidner and IBM do, however, teach a volatile memory.

The examiner takes official notice that it was well known to one of ordinary skill in the art at the time of invention to protect a volatile memory from data loss during normal operation.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine data protection with the volatile memory of Edwards, Bidner and IBM.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the volatile memory of Edwards, Bidner and IBM contains information necessary to provide insight into the functioning of the processor. Such information would necessarily benefit from the reliability that data protection offers.

Allowable Subject Matter

Claims 7, 8, 9, 10, 11, 13, 14, 20, 22, 33, 34, 35 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests wherein the overlay memory receives it address from an address counter that is incremented with each clock cycle that contains one of instruction information

and data information as outlined in claims 7 and 33. Prior art was not found that explicitly teaches both a debug interface and an existing serial communication port as outlined in claim 13. Prior art was not found that explicitly teaches each of another CPU, discrete gates, an FPGA and a DSP implementing the state machine as outlined in claims 14, 38 and 40. Prior art was not found that explicitly teaches or fairly suggests wherein the captured information is confined to a series of packets stored in the volatile memory as outlined in claim 20. Prior art was not found that explicitly teaches or fairly suggests wherein only the operational code and data of a CPU cycle are saved in the volatile memory and the state machine saves the address in a register when a trigger occurs as outlined in claim 22.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art not relied upon contains elements of the instant claims and/or represents a current state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 703-305-4622. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 703-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100